Docket No.: P2001,0119

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant

BERNHARD SELL ET AL.

Filed

CONCURRENTLY HEREWITH

Title

METHOD FOR FABRICATING A STORAGE CAPACITOR

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

- U.S. Patent No. 4,589,193 (Goth et al.), dated May 20, 1986;
- U.S. Patent No. 5,905,279 (Nitayama et al.), dated May 18, 1999;
- U.S. Patent No. 5,760,434 (Zahurak et al.), dated June 2, 1998;
- U.S. Patent No. 5,262,343 (Rhodes et al.), dated November 16, 1993;
- U.S. Patent Application Publication No. 2002/0125521 A1 (Schrems), dated September 12, 2002 and corresponding PCT WO 01/20681 A1 (Schrems), dated March 22, 2001;

European Patent Application EP 0 967 643 A2 (Gambino et al.), dated December 29, 1999;

European Patent Application EP 0 981 164 A2 (Bronner et al.), dated February 23, 2000;

European Patent Application EP 0 495 991 A1 (Takenaka), dated July 29, 1992;

PCT WO 01/17014 A1 (Sell et al.), dated March 8, 2001;

Patent Abstracts of Japan 63062371 (Akihiko), dated March 18, 1988;

Alperin, M. E. et al.: "Development of the Self-Aligned Titanium Silicide Process for VLSI Applications", IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 1, February 1985, pp. 61-69;

Yamada, K. et al.: "A Deep-Trenched Capacitor Technology for 4 Mega Bit Dynamic Ram", IEEE, IEDM 85, 29.3, pp. 702-705.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted

REG. NO. 29,308

LAURENCE A. GREENBERG

For Applicants

Date: August 26, 2003

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)											
Alperin, M. E. et al.: "Development of the Self-Aligned Titanium Silicide Process for VLSI Applications", IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 1, February 1985, pp. 61-69											
Yamada, K. et al.: "A Deep-Trenched Capacitor Technology for 4 Mega Bit											
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.											
	FOREIC DOCUMENT NO. 967 643 A2 981 164 A2 981 164 A2 101/17014 A1 CUMENTS (Included Process for VLSI And Pro	FOREIGN PATEN FOREIG	5/20/86 Goth et al. 5/905,279 5/18/99 Nitayama et al. 5/905,279 5/18/99 Nitayama et al. 5/905,279 Zahurak et al. 5/960,434 6/2/98 Zahurak et al. 5/962,343 11/16/93 Rhodes et al. 5/902/0125521 9/12/02 Schrems A1 COUNTRY DOCUMENT NO. DATE COUNTRY 0 967 643 A2 12/29/99 Europe 0 981 164 A2 2/23/00 Europe 0 495 991 A1 7/29/92 Europe 0 1/20681 A1 3/22/01 WIPO 0 1/17014 A1 3/8/01 WIPO CUMENTS (Including Author, Title, Date, Perocess for VLSI Applications", IEEE Journal of Ston, No. 1, February 1985, pp. 61-69 (Yamada, K. et al.: "A Deep-Trenched Capacitor Tolynamic Ram", IEEE, IEDM 85, 29.3, pp. 702-70 DATE CONSIDER	PATENT NO. DATE PATENTEE CLASS 4,589,193 5/20/86 Goth et al. 5,905,279 5/18/99 Nitayama et al. 5,760,434 6/2/98 Zahurak et al. 5,262,343 11/16/93 Rhodes et al. 2002/0125521 9/12/02 Schrems A1 Schrems FOREIGN PATENT DOCUMENT DOCUMENT NO. DATE COUNTRY CLASS 0 967 643 A2 12/29/99 Europe 0 981 164 A2 2/23/00 Europe 0 989 A1 7/29/92 Europe 0 11/20681 A1 3/22/01 WIPO 0 11/17014 A1 3/8/01 WIPO 0 11/17014 A1 3/8/01 WIPO CUMENTS (Including Author, Title, Date, Pertinent Patential Country of the Self-Aligned Titan Process for VLSI Applications", IEEE Journal of Solid-State Polynamic Ram", IEEE, IEDM 85, 29.3, pp. 702-705 DATE CONSIDERED citation considered, whether or not citation is in conforthrough citation if not in conformance and not considered.	PATENT NO. DATE PATENTEE CLASS CLASS 4,589,193 5/20/86 Goth et al. 5,905,279 5/18/99 Nitayama et al. 5,760,434 6/2/98 Zahurak et al. 5,262,343 11/16/93 Rhodes et al. 2002/0125521 9/12/02 Schrems A1 Schrems FOREIGN PATENT DOCUMENT DOCUMENT NO. DATE COUNTRY CLASS CLASS 0 967 643 A2 12/29/99 Europe 0 981 164 A2 2/23/00 Europe 0 981 164 A2 12/29/92 Europe 0 1/20681 A1 3/22/01 WIPO 0 1/17014 A1 3/8/01 WIPO 0 1/17014 A1 3/8/01 WIPO CUMENTS (Including Author, Title, Date, Pertinent Pages, etc. Decreases for VLSI Applications", IEEE Journal of Solid-State Circuits, 1/20, No. 1, February 1985, pp. 61-69 (Amada, K. et al.: "A Deep-Trenched Capacitor Technology for 4 Medynamic Ram", IEEE, IEDM 85, 29.3, pp. 702-705 DATE CONSIDERED Citation considered, whether or not citation is in conformance withrough citation if not in conformance and not considered. Inc	PATENT NO. DATE PATENTEE CLASS CLASS DA (1,589,193) 5/20/86 Goth et al. 5,905,279 5/18/99 Nitayama et al. 5,760,434 6/2/98 Zahurak et al. 6,262,343 11/16/93 Rhodes et al. 2002/0125521 9/12/02 Schrems A1 1/16/93 Schrems A1 1/16/93 CLASS CLASS TRAIL CLASS CLASS CLASS TRAIL CLASS CLASS TRAIL CLASS CLASS CLASS TRAIL CLASS CLASS CLASS CLASS TRAIL CLASS CLASS CLASS CLASS CLASS TRAIL CLASS TRAIL CLASS CLAS					

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